Design of Multi-layers DGS Resonator for Phase Noise Improvement of K-Band VCOs in 0.18 µm CMOS Technology

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***Abstract* — A novel technique for a low phase noise and compact K-band Voltage-Controlled Oscillator (VCO) using multi-layers DGS resonator is proposed. The proposed DGS resonator realizes an additional series resonance at the higher side of parallel resonance frequency, and this results in improving both the active and loaded quality factor of the resonator. The proposed resonator has active quality factor of 130 and a compact size of 0.009 mm² (0.000459 λ^2). Using the proposed DGS resonator in the VCO causes 9 dB improvement in the phase noise compared the VCO implemented using the conventional LC resonator. Two VCOs are designed using the method to illustrate the effect of the series resonance. The first VCO is designed three layers DGS resonator and the other VCO using two layers DGS resonator. The designs are implemented in 0.18 µm CMOS technology and consume 2.9 mW power, and from the post layout results, the first proposed VCO oscillates from 19.6 to 21.3 GHz (8.3 %) and has a phase noise of -113.2 dBc/Hz at 1 MHz offset frequency, and this results in the figure of merit (FoM) and FoM taking account of the tuning range to be -194.4 and -192.7 dB, respectively. The second VCO has a tuning range of 6.1 % and phase noise of -114 dBc/Hz @ 1 MHz offset at 19.6 GHz oscillation.**

Keywords* — *CMOS; DGS; K-band; finger capacitor; parallel resonator; Mos varactor; VCO.

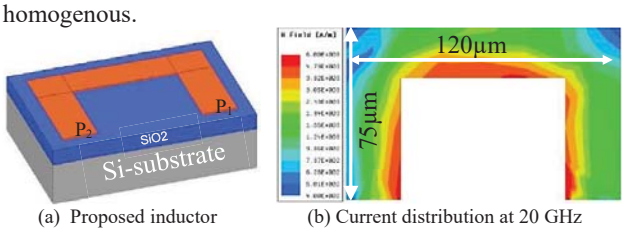
I. Introduction

Several techniques to improve the VCOs phase noise have been proposed by increasing the quality (Q-) factor of spiral inductors [1], [2]. Therefore, several efforts have been carried out to improve the Q-factor. One of them is to use a patterned ground shield (PGS) underneath the metal coil and the silicon substrate to reduce the substrate losses. [3]. Another method to improve the resonator quality factor, proposes using a defected ground structure (DGS) etched at the lowest metal layer, below a top layer 50 ohms microstrip. This method uses only one DGS layer and use another MIM capacitors in the resonator [5]. In [6], using a defected ground structure (DGS) resonator and a series capacitor to realize an additional series resonance and this method improves the phase noise by 3.8 dB compared to using of DGS resonator (single resonance).

In the proposed design we exploit all metal layers to implement the resonator without adding a MIM capacitors. In this manuscript, we first propose a new multilayer DGS structure to realize a high Q-factor parallel resonator in 0.18 µm CMOS technology and use it to design a low phase noise, wide band K-band VCO. The proposed design offers the following benefits; first, the parallel resonator is designed using 4 layers and has a small size that equals 0.000459 λ^2. Due to the series resonance generated, the proposed resonator enhances the VCO phase noise, as it has a high Q-factor. By using this resonator in oscillator circuits, the performance of the oscillator improved and its area reduced.

II. Proposed Parallel Resonator

The proposed K-band parallel resonator is implemented using the top metal layer M_6 (inductor), and lower layers M_4, M_3 and M_2 to form the capacitor. Fig. 1 shows the structure of proposed inductor, and its current distribution at 20 GHz. The dimension of the proposed inductor is 0.12 mm x 0.075 mm. The current distribution across the inductor surface is homogenous.



(a) Proposed inductor (b) Current distribution at 20 GHz

Fig. 1. Proposed inductor and its current distribution.

High Frequency Structure Simulator (HFSS) by ANSYS Inc. is employed to simulate the proposed inductor and the differential inductance and quality factor are calculated from the S-parameters using the following two equations. Fig. 2 illustrates the inductance and quality factor; the differential inductance is close to 0.14 nH with a quality factor of 35 in the K-band.

$$L = \frac{Im\left(\frac{4}{Y_{11}+Y_{22}-Y_{12}-Y_{21}}\right)}{2\pi f} \quad (1)$$

$$Q = \frac{Im\left(\frac{4}{Y_{11}+Y_{22}-Y_{12}-Y_{21}}\right)}{Re\left(\frac{4}{Y_{11}+Y_{22}-Y_{12}-Y_{21}}\right)} \quad (2)$$

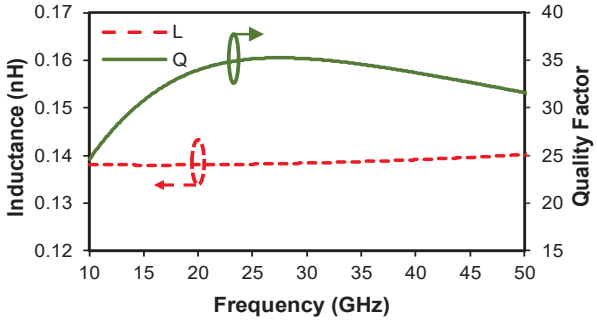
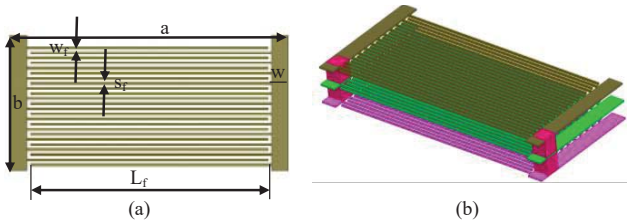


Fig. 2. Differential inductance and quality factor of the proposed inductor.

In the proposed resonator, the capacitor is designed in the lower layers and has the shape of a finger capacitor. First, design the finger capacitor in layer 4 then add another capacitor in layer 3 and layer 2 so the total capacitance we can have from those three layers is about 110 fF. The structure of the finger capacitor is displayed in Fig. 3. The dimension of the finger capacitor is shown in table I.



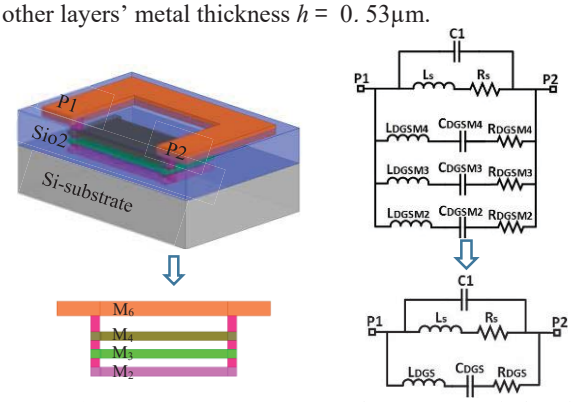
(a) (b)

Fig. 3. Finger capacitor structure (a) M4 layer finger capacitor and (b) M4, M3 and M2 layers finger capacitor.

TABLE I. DESIGN PARAMETERS FINGER CAPACITOR

Parameters	*a*	*B*	L_f	w_f	s_f	*w*
Dimension (μm)	82	40	71	0.5	1	5

The parallel resonator is designed by combining the U-shaped inductor parallel to the finger capacitors as illustrated in Fig. 4. The equivalent circuit of the DGS resonator is cleared in Fig. 5 which consists of an inductor L_s, loss resistance R_s and coupling capacitor C_1, and three capacitors in parallel layer 4, layer 3 and layer 2. The designed parallel resonator using DGS is shown in fig. 4, as BSF on Si substrate with ε_r = 4, thickness 200μm, M_6 metal thickness h_{M6} = 2.34μm, and other layers' metal thickness h = 0. 53μm.



(a) DGS resonator (b)Resonator equivalent circuit

Fig. 4. Proposed DGS resonator and its equivalent circuit where L_s=0.14nH, R_s=0.6Ω, C_1=20fF, L_{DGS}=0.085nH, C_{DGS}=110fF, R_{DGS}=2.3 Ω.

Fig. 5 shows that by adding more DGS layers not only the resonance frequency of the resonator is shifted down, but also the loaded quality factor in increased. Also, the loaded quality factor using this DGS resonator is soared from 2.2 to 4.7 in a comparison with the offered LC resonator as clear in Fig. 6. Table II illustrates the loaded quality factor in the different cases of DGS and in the conventional (offered) resonator where the loaded quality factor (Q_{loaded}) is calculated by:

$$Q_{loaded} = \frac{f_c}{BW} \tag{3}$$

TABLE II. LOADED QUALITY FACTOR USING DIFFERENT DGS LAYERS

Parameters	C_{DGS} (fF)	Q_{loaded}
M_4 Capacitor	45 fF	3.9
M_4 M_3 Capacitor	85 fF	4.3
M_4 M_3 M_2 Capacitor	110 fF	4.7
Conventional LC resonator		2.2

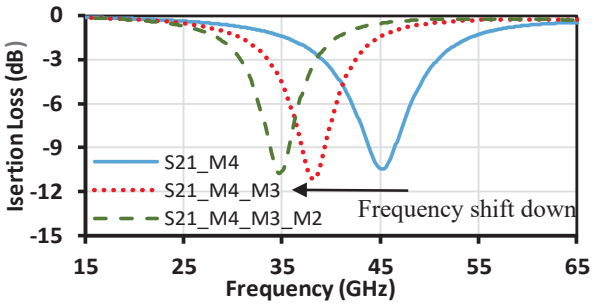


Fig. 5. Effect of adding more DGS layers on the insertion loss of the resonator.

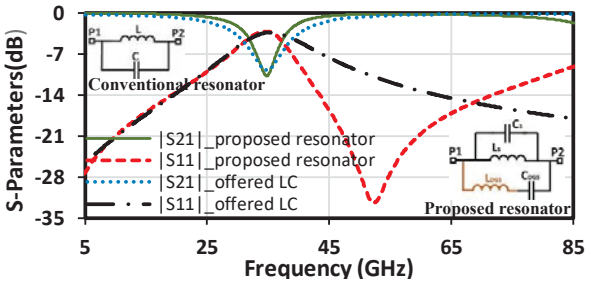


Fig. 6. Simulated S-parameters of the proposed resonator and offered LC circuit in the technology.

The S-parameters of the proposed resonator and its equivalent circuit are illustrated in Fig. 7 and there is an agreement between the response of the resonator and its equivalent circuit. Also, from the S-parameters curve, there are two resonances frequencies, the series resonance frequency (f_s) and is generated from DGS and the parallel resonance (f_0) and comes from the parallel combination DGS and inductor. For the proposed DGS resonator, (4) we can express the susceptance of the equivalent circuit. When the susceptance equals zero the parallel resonance occurs while if the susceptance is infinite the series resonance happens [7].

$$B = \frac{(1-\omega^2 L_{DGS}C_{DGS})(\omega^2 C_1 L_s - 1)+\omega^2 L_s C_{DGS}}{\omega L_s(1-\omega^2 L_{DGS}C_{DGS})} \tag{4}$$

B=0;

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{L_s(C_1+C_{DGS})+L_{DGS}C_{DGS}}{C_1 C_{DGS} L_s L_{DGS}}} \tag{5}$$

B=∞;

$$f_s = \frac{1}{2\pi}\frac{1}{\sqrt{L_{DGS}C_{DGS}}} \tag{6}$$

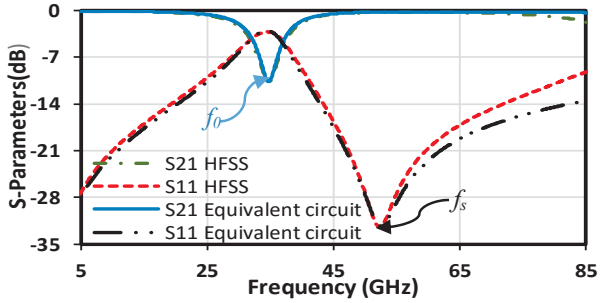


Fig. 7. Comparison of the equivalent circuit and EM-simulated s-parameters for the parallel DGS resonator.

The noise spectrum of the VCO depends on the active Q factor (Q_K) of the resonator, which can be calculated using (7) [7], where P_0 is the power observed when the noise source is solely connected to the load R_L.

$$Q_K = \frac{\omega_0}{2}\left|\frac{Y'(\omega_0)}{Y(\omega_0)}\right| \quad (7)$$

$$P(\omega) = \left(\frac{\omega_0}{2Q_K\Delta\omega}\right)P_0 \quad (8)$$

The simulated active Q-factor of the proposed DGS resonator in the case of using (M_4, M_4M_3, $M_4M_3M_2$) and the conventional resonator (the offered LC from technology) are shown in Fig 8. The proposed VCO possess higher active Q-factor and it increased by 44 % compared to the conventional resonator.

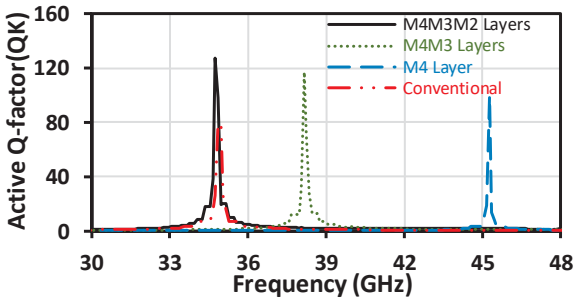


Fig. 8. Simulated active Q-factor of the proposed DGS resonator and the conventional resonator.

III. Circuit Design

Fig. 9 illustrates the schematic of the proposed PN-VCO. It consists of a cross-coupled NMOS pair ($M_{1\text{-}2}$), a cross-coupled PMOS pair ($M_{3\text{-}4}$), current source (M_5), a feedback capacitor (C_f, C_1) to increase the negative transconductance, parallel resonator, varactor capacitor C_v. The control voltage $V_{Control}$ is used to fine tune the oscillation frequency at the high/low frequency band. The VCO core is followed by an output buffer. In the first half cycle of the oscillation, the transistors M_4 and M_1 are in the on state, M_3 and M_2 are in the off state, the current passes through the multi-layer resonator from left to right, in the second half cycle the current direction in the resonator is opposite from right to left. The two feedback capacitors C_1 and C_f, supply an additional negative $-G_m$ to the LC tank, which is denoted as $n*g_m$, where n is the capacitive feedback ratio $n = C_1/(C_1+C_f)$ and g_m is the trans-conductance of the transistors [8]. The total negative conductance is generated from the cross-coupled connection and the capacitive feedback together; consequently, high $-G_{neg}$ could enhance the phase noise and reduce the power consumption. The simplified equivalent circuit of the VCO with DGS resonator is shown in Fig. 9. The generated negative conductance (G_{neg}) and the oscillation frequency of the VCO (ω_{osc}) can be calculated using:

$$G_{neg} = -2 * g_m(1 + 2 * n) \quad (9)$$

$$\omega_{osc} = \frac{1}{\sqrt{L_s*(C_{DGS}+C_t)}} \quad (10)$$

where g_m is the transconductance of the transistors, C_t is the varactor capacitance, feedback capacitors and parasitic capacitance of transistors.

MOS Varactors are used to tune the oscillation frequency, in the proposed VCO. Fig. 10 illustrates the capacitance and the quality factor of MOS varactor with and without the series capacitor that improves the quality factor and consequently enhances the phase noise. By improving the quality factor of the Mos varactors using series capacitor the phase noise of the VCO is improved by 7 dB as shown in Fig. 11.

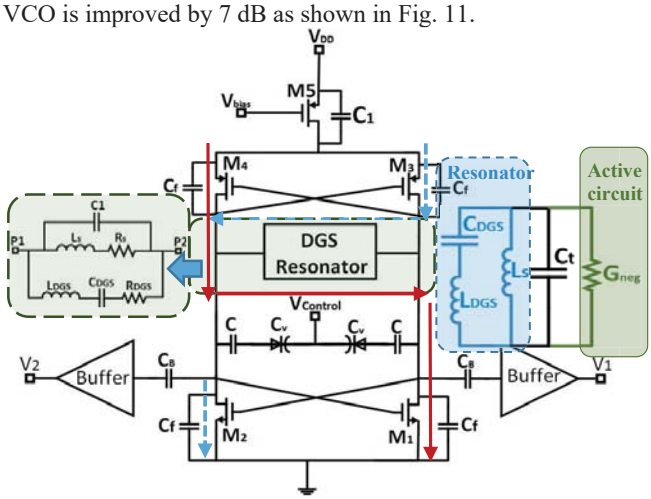


Fig. 9. Schematic of the proposed VCO using DGS resonator.

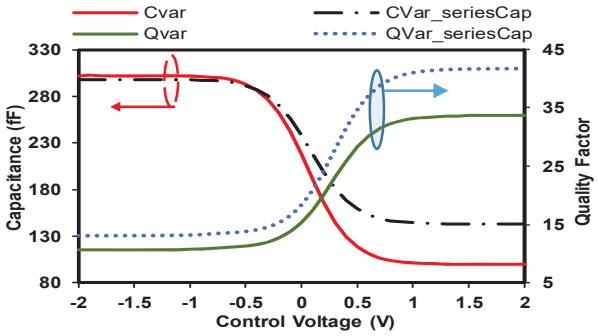


Fig. 10. Comparison between the capacitance and quality factor of MOS varactors with and without series capacitor.

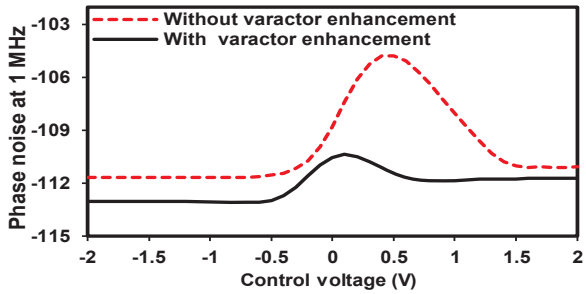
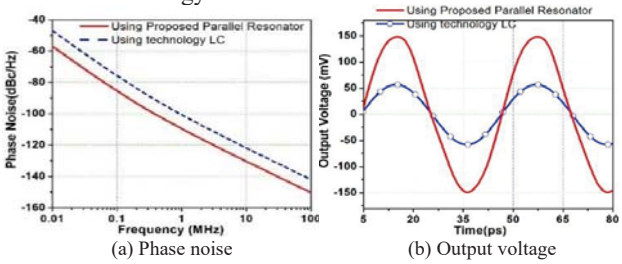


Fig. 11. Phase noise improvement due to the series capacitor.

Using the DGS resonator the circuit oscillates at frequency of 23.7 GHz. Fig. 12 shows that the proposed resonator improves the phase noise by 9 dB, moreover the output power increases by 8.3 dB in a comparison with the offered LC circuit from the technology.



(a) Phase noise (b) Output voltage

Fig. 12. Phase noise and output voltage of the oscillator in the case of the proposed DGS resonator and the offered LC circuit from the technology.

IV. Layout and Simulation Results

The layout of the proposed VCO is displayed in Fig. 13. The total chip area is 0.264 mm^2 including the two output buffers, while the VCO core occupies an area of 0.0356 mm^2. The DC power consumption of the wide band VCO is 2.9 mW from a supply voltage of 1.5 V. The first VCO achieves frequency tuning range from 19.56 to 21.24GHz (8.24 %) as shown in Fig. 14 and the phase noise at 1MHz offset from -113.2 to -110.6 dBc/Hz. The second proposed design is planned to use M_3M_2 DGS resonator and increase the feedback capacitor (C_f) to enhance the phase noise by 1 dB as clear in Fig.15.

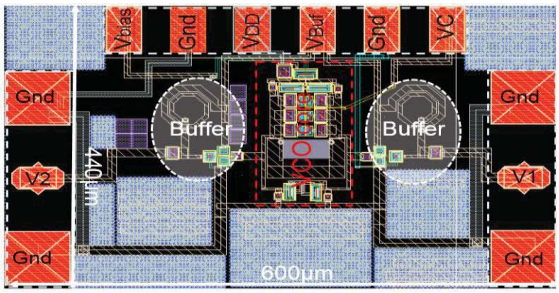


Fig. 13. Layout of the proposed VCO.

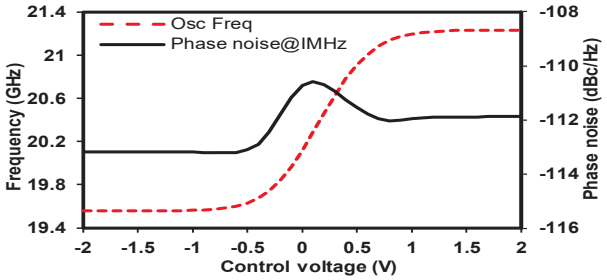


Fig. 14. Frequency tuning range and phase noise of the proposed VCO.

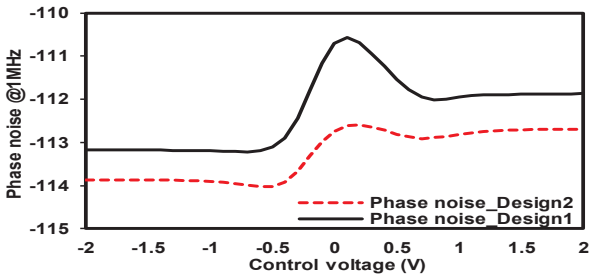


Fig. 15. Phase noise of the proposed design 1 and design 2.

The proposed VCOs display better or comparable performances compared to reported VCOs concerning phase noise, power consumption, area, frequency tuning range, FoM and FoM^T, as illustrated in Table III.

V. Conclusion

A novel method to realize a low phase noise and compact size K-band VCO in 0.18 µm CMOS technology is presented. By using a DGS resonator (multi -layers) as high- Q factor LC tank circuit, the performance of the VCO is enhanced, the VCO size is reduced and the phase noise is improved by 9 dB compared to conventional resonator. The developed VCOs achieve wide tuning range (8.3 % and 6.1 %) while maintaining low-power consumption. The proposed VCOs demonstrate FoM and FoM^T of -194.4, -195.2 and -192.7, -190.1 dBc/Hz, respectively, and occupies the smallest area of 0.0356 mm^2.

Table III. Performance Conparison of K-Band VCOs

Reference	[6]*	[9]	[10]	[11]	VCO1*	VCO2*
Technology [µm]	0.18	0.18	0.13	0.18	0.18	0.18
F_{osc} [GHz]	21	25	19.5	18.95	20	19.8
FTR[%]	3.4	2.4	4.8	3.38	8.3	6.1
P_{DC} [mW]	7.5	13.2	5	3.3	2.94	2.94
PN@1MHz [dBc/Hz]	-111.9	-104	-103.1	-110.8	-113.2	-114.03
Area [mm^2]	N.A	0.4	0.3	0.24	0.0356	
FoM[dBc/Hz]	-188.7	-180	-181	-191.2	-194.4	-195.2
FoM^T[dBc/Hz]	-178.3	-167.6	-175	-182.3	-192.7	-190.1

*Post layout, $\mathrm{FoM} = \mathrm{PN} - 20\log(f_{osc}/\Delta f) + 10\log(\mathrm{P_{DC}})$,

and $\mathrm{FoM^T} = \mathrm{FoM} - 20\log(FTR/10)$

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